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| EXAMINER | |
|---|---|
| FLANDERS, ANDREW C | |
| ART UNIT | PAPER NUMBER |
| 2644 | |

DATE MAILED: 02/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/621,504 | MALLINSON, MARTIN | |
| | Examiner | Art Unit | |
| | Andrew C. Flanders | 2644 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *09 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-3,5-46 and 48-85* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *43-46 and 71-85* is/are allowed.

6)☒ Claim(s) *1,8-10,12-24,31-42,48-53,57-60,62 and 64-68* is/are rejected.

7)☒ Claim(s) *2,3,5-7,11,25-30,54-56,61,63,69 and 70* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 September 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Response to Arguments*

Applicant's arguments, filed 09 December 2005, with respect to the rejection(s) of the claim(s) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made as stated below.

### *Claim Objections*

Applicant is advised that should claim 50 be found allowable, claim 73 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

### *Claim Rejections - 35 USC § 112*

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

**Claim 62** rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The term "substantially small range of pulses in time" in claim 62 is a relative term which renders the claim indefinite. The term "substantially small range of pulses in time" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. Appropriate correction is required.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

**Claims 24, 31 and 34** are rejected under 35 U.S.C. 102(a) as being anticipated by Midya (U.S. Patent 5,04,427).

Regarding **Claim 24**, Midya discloses:

A digital signal processing circuit (Fig. 1) comprising:

a pulse width modulator having an output with a distortion (Fig. 1 element 14); and

means for sampling said output and suppressing said distortion in a digital domain (Fig. 1 element 16).

Regarding **Claims 31**, in addition to the elements stated above regarding claim 24, Midya further discloses:

An integrated circuit chip comprising the signal processor of claim 24 (i.e. the compensation method and apparatus taught herein is very suitable for integration into a single integrated circuit; col. 6 lines 20 – 30).

Regarding **Claim 34**, in addition to the elements stated above regarding claim 124, Midya further discloses:

An audio power amplification system comprising the signal processor of claim 1 (Fig. 1).

**Claim 24** is rejected under 35 U.S.C. 102(b) as being anticipated by Oprescu (U.S. Patent 6,208,279).

Regarding **Claim 24**, Oprescu discloses:

A digital signal processing circuit (Fig. 1) comprising:

a pulse width modulator having an output with a distortion (Fig. 1 element 20); and

means for sampling said output and suppressing said distortion in a digital domain (Fig. 1 element 30).

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

**Claims 1, 8, 9, 23 and 42** are rejected under 35 U.S.C. 103(a) as being unpatentable Oprescu (U.S. Patent 6,208,279).

Regarding **Claims 1 and 23**, Oprescu discloses:

A signal processor comprising:

a pulse width modulator having a clock rate (i.e. Fig. 5 element 101); and

a digital filter configured to receive an output of said pulse width modulator, wherein said output comprises a distortion, and wherein said digital filter samples said output to suppress said distortion (i.e. Fig. 5 element 102; digital signals Y(k) are produced by modulator 20 at a frequency Fs and represents the pulse-modulated input signal together with any quantization noise, out-of-band components, circuit noise, and

interference that may be included in the analog signal. As pulses in signal Y(k) propagate through the digital filter, quantization noise is attenuated...; col. 4 lines 25 – 33)

Oprescu does not explicitly discloses that the digital filter samples said output at said clock rate to suppress said distortion.

Oprescu does discloses two clock rates for the modulator and digital filter (shown as ClkM (modulator) and ClkF(filter)). Further Oprescu discloses the analog input signal V(t) is sampled at a very high rate as directed by the clock signal ClkM produced by the system control and Modulator 20 generates a series of digital one-bit output samples Y(k); col. 3 lines 55 – 60; each of these pulses Y(k) are then multiplied in the digital filter every clock cycle; col. 4 lines 50 - 67. Thus while not explicitly disclosed that ClkM is equal to ClkF, these two clock rates are not dependent upon each other and can be set to be equal as the number of instructions/operations per cycle are not limited by the disclosure. As further evidence please see Menkhoff (U.S. Patent 6,137,349) which discloses a digital signal source coupled to a digital LPF which is closed at the same clock rate (Fig. 1 elements f1, 1, 5 and 7)

It would have been obvious to one of ordinary skill in the art at the time of the invention to set these two clocks to equal values. One would have been motivated to do so to create a synchronous digital circuit. A synchronous digital circuit is desirable because the operation of the circuit can be predicted exactly (see the wikipedia.com definition of synchronous circuit).

Regarding **Claim 8**, in addition to the elements stated above regarding claim 1, Oprescu fails to explicitly disclose wherein said digital filter comprises an IIR filter.

However, Examiner takes official notice that IIR filters are well known in the art. Further, Oprescu discloses a FIR filter. It would have been obvious to one of ordinary skill in the art at the time of the invention to substitute a IIR filter in place of an FIR filter. One would have been motivated to do so in order to achieve a given filtering characteristic using less memory and calculations than a similar FIR filter; see dspGuru reference, section 1.4.

Regarding **Claim 9**, in addition to the elements stated above regarding claim 8, Oprescu fails to explicitly disclose wherein said IIR filter comprises a single pole filter.

However, filters with various pole arrangements (in particular a single pole filter) are notoriously well known in the art. Arranging a filter such as the modifications IIR filter with a single pole configuration would have been obvious. Various pole placements provide various responses and depending on the desired response, a specific arrangement (a single pole in the instant case) can be designed and implemented.

Regarding **Claim 42**, in addition to the elements stated above regarding claim 24, Oprescu fails to explicitly disclose wherein said sampling occurs at a clock rate of said pulse width modulator.

Oprescu does discloses two clock rates for the modulator and digital filter (shown as ClkM (modulator) and ClkF(filter)). Further Oprescu discloses the analog input signal V(t) is sampled at a very high rate as directed by the clock signal ClkM produced by the system control and Modulator 20 generates a series of digital one-bit output samples Y(k); col. 3 lines 55 – 60; each of these pulses Y(k) are then multiplied in the digital filter every clock cycle; col. 4 lines 50 - 67. Thus while not explicitly disclosed that ClkM is equal to ClkF, these two clock rates are not dependent upon each other and can be set to be equal as the number of instructions/operations per cycle are not limited by the disclosure. As further evidence please see Menkhoff (U.S. Patent 6,137,349) which discloses a digital signal source coupled to a digital LPF which is closed at the same clock rate (Fig. 1 elements f1, 1, 5 and 7)

It would have been obvious to one of ordinary skill in the art at the time of the invention to set these two clocks to equal values. One would have been motivated to do so to create a synchronous digital circuit. A synchronous digital circuit is desirable because the operation of the circuit can be predicted exactly (see the wikipedia.com definition of synchronous circuit).

**Claims 15 - 20 and 36 - 41** are rejected under 35 U.S.C. 103(a) as being unpatentable over Oprescu (U.S. Patent 6,208,279) in view of Terui (U.S. Patent 5,903,871).

Regarding **Claims 15 and 36**, in addition to the elements stated above regarding claims 1 and 24, Oprescu fails to disclose the limitations of claims 15 and 36. Terui discloses a portable audio player (entire document) (i.e. a portable audio player).

One of ordinary skill in the art at the time of the invention would have been motivated to use the device in a portable device such as Terui's hand held recorder and playback device to include an A/D converter with reduced complexity that minimizes power consumption; col. 2 lines 35 – 50; as it is desirable to minimize power consumption, size and complexity in portable environments.

Regarding **Claims 16 and 37**, in addition to the elements stated above regarding claims 15 and 36, the combination of Oprescu and in view of Terui further discloses a recording medium for storing digital audio data (col. 4 lines 50 - 59) (i.e. a digital audio signal source).

Regarding **Claims 17, 18, 38, and 39**, in addition to the elements stated above regarding claims 15 and 36, the combination of Oprescu and in view of Terui further discloses the main recording medium portion uses a magneto- optical disc (col. 5 lines 3 - 4) (i.e. an optical disk reader).

Regarding **Claims 19 and 40**, in addition to the elements stated above regarding claims 16 and 37, the combination of Oprescu and in view of Terui further discloses a

recording medium for storing digital audio data (col. 4 lines 50 - 59) (i.e. a memory for storage of a digital audio file).

Regarding **Claims 20 and 41**, in addition to the elements stated above regarding claims 16 and 37, the combination of Ruha in view of Oprescu and in further view of Terui further discloses that the recording medium receives digital audio from the main control circuit (col. 4 lines 50 - 59) (i.e. wherein said digital audio signal source comprises a digital receiver).

**Claims 1, 10, 12 – 14, 21 – 23, 32, 33, 42 and 48** are rejected under 35 U.S.C. 103(a) as being unpatentable Midya (U.S. Patent 6,208,279).

Regarding **Claims 1 and 23**, Midya discloses:

A signal processor comprising:

a pulse width modulator having a clock rate (i.e. Fig. 1 element 14); and

a digital filter configured to receive an output of said pulse width modulator, wherein said output comprises a distortion, and wherein said digital filter samples said output to suppress said distortion (Fig. 1 element 15).

Midya does not explicitly discloses that the digital filter samples said output at said clock rate to suppress said distortion.

However, digital processing circuits typically include a clock to perform instructions at a given rate. it would have been obvious to one of ordinary skill in the art at the time of the invention to set the device disclosed in Fig.1 to have equal clock values. As further evidence please see Menkhoff (U.S. Patent 6,137,349) which discloses a digital signal source coupled to a digital LPF which is closed at the same clock rate (Fig. 1 elements f1, 1, 5 and 7). One would have been motivated to do so to create a synchronous digital circuit. A synchronous digital circuit is desirable because the operation of the circuit can be predicted exactly (see the wikipedia.com definition of synchronous circuit).

Regarding **Claim 10**, in addition to the elements stated above regarding claim 1, Midya further discloses:

wherein said digital filter further comprises a low pass filter (col. 2 lines 44 – 47).

Regarding **Claim 12**, in addition to the elements stated above regarding claim 1, Midya further discloses:

An integrated circuit chip comprising the signal processor of claim 1 (i.e. the compensation method and apparatus taught herein is very suitable for integration into a single integrated circuit; col. 6 lines 20 – 30).

Regarding **Claims 13, 14, 32 and 33**, in addition to the elements stated above regarding claims 12 and 31, Midya does not explicitly disclose wherein said system provides a two-channel or eight-channel output. Midya does disclose a digital audio input in the form of a digital source in element 12 of Fig. 1. Digital audio sources are well known to contain multiple channels such as 2 or 8. It would have been obvious to one of ordinary skill in the art to modify Midya to enable the invention to output multiple channels thus allowing the invention to operate with many well known audio signals.

Regarding **Claim 21**, in addition to the elements stated above regarding claim 1, Midya further discloses:

An audio power amplification system comprising the signal processor of claim 1 (Fig. 1).

Regarding **Claims 22 and 35**, in addition to the elements stated above regarding claims 21 and 34, Midya fails to explicitly disclose an RC type demodulation filter.

Midya does disclose a low pass filter connected to the output. It is notoriously well known in the art that low pass filters can be constructed with simple resistors and capacitors thus forming an RC type demodulation filter.

Regarding **Claim 42**, in addition to the elements stated above regarding claim 24, Midya fails to explicitly disclose wherein said sampling occurs at a clock rate of said pulse width modulator.

However, digital processing circuits typically include a clock to perform instructions at a given rate. it would have been obvious to one of ordinary skill in the art at the time of the invention to set the device disclosed in Fig.1 to have equal clock values. As further evidence please see Menkhoff (U.S. Patent 6,137,349) which discloses a digital signal source coupled to a digital LPF which is closed at the same clock rate (Fig. 1 elements f1, 1, 5 and 7). One would have been motivated to do so to create a synchronous digital circuit. A synchronous digital circuit is desirable because the operation of the circuit can be predicted exactly (see the wikipedia.com definition of synchronous circuit).

Regarding **Claim 48**, Midya discloses:

An integrated circuit chip configured to generate a pulse width modulated digital output signal (i.e. Fig. 1 element 14 and the compensation method and apparatus taught herein is very suitable for integration into a single integrated circuit; col. 6 lines 20 – 30),

wherein the output signal has a distortion, and wherein said distortion is suppressed by a digital filter (Fig. 1 element 15).

Midya fails to explicitly disclose receiving a pulse code modulated digital signal and that the digital filter operates at at least a clock rate of said pulse width modulated digital signal.

However, digital processing circuits typically include a clock to perform instructions at a given rate. it would have been obvious to one of ordinary skill in the art

at the time of the invention to set the device disclosed in Fig.1 to have equal clock values. As further evidence please see Menkhoff (U.S. Patent 6,137,349) which discloses a digital signal source coupled to a digital LPF which is closed at the same clock rate (Fig. 1 elements f1, 1, 5 and 7). One would have been motivated to do so to create a synchronous digital circuit. A synchronous digital circuit is desirable because the operation of the circuit can be predicted exactly (see the wikipedia.com definition of synchronous circuit).

Furthermore, Midya does disclose receiving an digital audio source (Fig. 1 element 12). It is well known in the art that pulse code modulated digital audio sources exist (i.e. a Compact Disc is typically encoded with PCM data). Thus it is obvious that if the digital source was a compact disc or some other form of PCM encoded digital audio data, the system would be configured to receive a pulse code modulated digital signal. It would have been obvious to one of ordinary skill in the art at the time of the invention to configure the invention disclosed by Midya to accept PCM audio data. One would have been motivated to do so to allow the system to work with a notoriously well known form of digital audio data that is commonly available (i.e. a PCM encoded Compact Disc).

**Claim 49 – 53, 57 – 60, 62 and 64 – 68** are rejected under 35 U.S.C. 103(a) as being unpatentable Midya (U.S. Patent 6,208,279) in view of Botti (U.S. Patent 6,594,309).

Regarding **Claims 49 and 68**, Midya discloses:

A method comprising

modulating a signal into a third signal comprising a plurality of pulses in time having a clock rate (i.e. element 14 of Fig. 1 modulates a digital signal into a PWM input to the correction stage)

filtering in a digital domain said plurality of pulses in time to suppress a distortion in said third signal (i.e. Fig. 1 element 15).

Midya doesn't explicitly disclose modulating a first pulse code modulated signal having a first resolution into a second pulse code modulated signal having a second resolution, wherein said second resolution is smaller than said first resolution or that the second pulse code modulated signal is the signal modulated to a third signal.

Botti discloses modulating a first pulse code modulated signal having a first resolution into a second pulse code modulated signal having a second resolution, wherein said second resolution is smaller than said first resolution (Fig. 1 and each digital M bit word is converted by oversampling and noise shaping techniques into an N bit word of a lower number of bits than the input word (M>N); col. 3 lines 32 – 37).

Furthermore, Midya does disclose receiving an digital audio source (Fig. 1 element 12). It is well known in the art that pulse code modulated digital audio sources exist (i.e. a Compact Disc is typically encoded with PCM data). Thus it is obvious that if the digital source was a compact disc or some other form of PCM encoded digital audio data, the system would be configured to receive a pulse code modulated digital signal. It would have been obvious to one of ordinary skill in the art at the time of the invention

to configure the invention disclosed by Midya to accept PCM audio data. One would have been motivated to do so to allow the system to work with a notoriously well known form of digital audio data that is commonly available (i.e. a PCM encoded Compact Disc).

Applying the teachings of Botti to the Digital Source of Midya, when a compact disc encoded with PCM data is present would read on modulating said second pulse code modulated signal into a third signal comprising a plurality of pulses in time having a clock rate.

It would have been obvious to one of ordinary skill in the art at the time of the invention to add the teachings of Botti to the invention taught by Midya. One would have been motivated to do so to avoid problems with harmonic distortion, linearity and signal residues in a 16 bit 44.1 kHz PCM signal; Botti col. 3 lines 55 – 65.

Regarding **Claims 50 and 73**, in addition to the elements stated above regarding claim 49, the combination further discloses:

wherein said first resolution is between 12 bits and 24 bits inclusively (i.e. a 16 bit PCM signal as taught by Botti)

Regarding **Claim 51**, in addition to the elements stated above regarding claim 50, the combination further discloses:

wherein said first resolution is 16 bits (i.e. a 16 bit PCM signal as taught by Botti).

Regarding **Claim 52 and 53**, in addition to the elements stated above regarding claim 50, the combination fails to explicitly discloses wherein said second resolution is between 2 and 6 bits inclusively or wherein the second resolution is 4 bits. However, Botti discloses that the output length N is less than the input length M and this bit ranges of 2 – 6, and a setting of 4 bits are made obvious as Botti's input is 16 bits. An input of 16 bits would result in an output of 1 to 15 bits. This range includes 2 – 6 bits and 4 bits as claimed by Applicant. Choosing this exact range does not provide any unexpected results and thus is a design choice by Applicant.

Regarding **Claim 57**, in addition to the elements stated above regarding claim 49, the combination further discloses:

wherein said filtering comprises using digital filter (i.e. Fig. 1 element 15 in Midya; and the digital correction stage can include a low pass filter; col. 2 lines 45 - 50).

Regarding **Claim 58**, in addition to the elements stated above regarding claim 57, the combination fails to explicitly disclose wherein said digital filter comprises an IIR filter.

Midya does disclose a low pass filter as part of the digital correction stage; col. 2 lines 45 – 50. It would have been obvious to one of ordinary skill in the art at the time of the invention to use an IIR filter as the low pass filter implementation. One would have been motivated to do so in order to achieve a given filtering characteristic using less memory and calculations; see dspGuru reference, section 1.4.

Regarding **Claim 59**, in addition to the elements stated above regarding claim 58, the combination fails to explicitly disclose wherein said digital filter comprises a single pole filter.

However, Low pass single pole filters are notoriously well known in the art; as is evidenced by Lis (U.S. Patent Application Publication 2004/0037432) in paragraph 31. Depending on the response desired, various pole arrangements (in particular a single pole filter) are notoriously well known in the art. Arranging a filter such as the modifications IIR filter with a single pole configuration would have been obvious. Various pole placements provide various responses and depending on the desired response, a specific arrangement (a single pole in the instant case) can be designed and implemented.

Regarding **Claim 60**, in addition to the elements stated above regarding claim 57, the combination further discloses:

wherein said digital filter comprises a low pass filter (i.e. the correction stage may include a low pass filter; col. 2 lines 45 – 50 in Midya).

Regarding **Claim 62**, in addition to the elements stated above regarding claim 49, the combination further discloses:

wherein said plurality of pulses in time is a substantially small range of pulses in time (i.e. Fig. 1 element 14 outputs a digital pulse modulated input which is a plurality of pulses in time)

Regarding **Claim 64**, in addition to the elements stated above regarding claim 49, the combination fails to explicitly disclose wherein said filtering comprises sampling at said clock rate.

However, digital processing circuits typically include a clock to perform instructions at a given rate. It would have been obvious to one of ordinary skill in the art at the time of the invention to set the device disclosed in Fig.1 to have equal clock values. As further evidence please see Menkhoff (U.S. Patent 6,137,349) which discloses a digital signal source coupled to a digital LPF which is closed at the same clock rate (Fig. 1 elements f1, 1, 5 and 7). One would have been motivated to do so to create a synchronous digital circuit. A synchronous digital circuit is desirable because the operation of the circuit can be predicted exactly (see the wikipedia.com definition of synchronous circuit).

Regarding **Claim 65**, in addition to the elements stated above regarding claim 49, the combination further discloses:

amplifying said third signal to produce an amplified output (Fig. 1 element 18 in Midya).

Regarding **Claim 66**, in addition to the elements stated above regarding claim 65, the combination further discloses:

creating an analog signal from said amplified output (Fig. 1 element 19 in Midya).

Regarding **Claim 67**, in addition to the elements stated above regarding claim 66, the combination fails to explicitly disclose wherein said creating comprises using an RC filter circuit.

However, Midya does disclose a low pass filter connected to the output. It is notoriously well known in the art that low pass filters can be constructed with simple resistors and capacitors thus forming an RC type demodulation filter.

***Allowable Subject Matter***

Claims 43 – 46 and 71 - 85 are allowed.

Claim 2, 3, 5 – 7, 11, 25 – 30, 54 – 56, 61, 63, 69 and 70 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in

independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Claims 2 and 25 claim an oversampling modulator upstream of and coupled to said pulse width modulator. Neither Midya nor Oprescu discloses this limitation. Ruha discloses an oversampling modulator upstream of a pulse width modulator (Fig. 4) and Masuda discloses one as well (Fig. 4). However, it would not have been obvious to one of ordinary skill in the art to apply the teachings of Masuda or Ruha to add an oversampling modulator to the circuits disclosed by Midya and Oprescu as there are no disclosed advantages for using one nor was the knowledge known in the art to use one.

Claims 11 and 61 discloses the signal processor further comprising a feedback path comprising said digital filter. The prior art does not explicitly disclose the claimed digital filter in feedback loop. Feedback paths are notoriously well known in the art, however, implementing one in the prior art cited would not have been obvious to one of ordinary skill in the art as there are no disclosed or apparent advantages.

Claim 54 discloses wherein said modulation said first pulse code modulated signal comprises using a sigma-delta type modulator. Oversampling using a sigma

delta type modulator is well known in the art as is evidenced by Ruha (U.S. Patent 6,466,087) in col. 4 lines 23 – 32. However, It would not have been obvious to one of ordinary skill in the art at the time of the invention to substitute Ruha's over sampler in place of the disclosed in Fig. 1 by Botti as there are no discloses or apparent advantages for doing so.

## *Conclusion*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew C. Flanders whose telephone number is (571) 272-7516. The examiner can normally be reached on M-F 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sinh Tran can be reached on (571) 272-7546. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

acf

XU MEI
PRIMARY EXAMINER